

## CLAIMS

What is claimed is:

1    1.    A method of testing a semiconductor chip having a plurality of common I/Os  
2    associated therewith whose characteristics or properties may be tested by applying a test  
3    signal through a control I/O, the method comprising the steps of:

4                 performing a chip-to-package connectivity test upon at least one of the common  
5    I/O through the control I/O; and  
6                 determining whether the common I/O is faulty from a result of the chip-to-  
7    package connectivity test.

1    2.    The method of claim 1, wherein performing a pin-to-package connectivity test  
2    comprises:

3                 launching a transition through the common I/O to an associated I/O package  
4    connection and pad; and  
5                 observing a response of the transition.

1    3.    The method of claim 2, further comprising: triggering a first latch at an  
2    initialization of the transition response and triggering a second latch when the transition  
3    response has reached a transition threshold value.

1    4.    The method of claim 3, wherein determining whether the chip-to-package  
2    connection is faulty comprises: comparing a difference between values stored in  
3    association with the first and second latches.

1       5.     The method of claim 1, wherein determining whether the chip-to-package  
2 connection is faulty comprises: comparing a first RC constant associated with a first  
3 signal relating to a connectivity test of a first I/O with a second RC constant associated  
4 with a second signal relating to a connectivity test of a second I/O.

1       6.     The method of claim 5, further comprising identifying the first I/O as having a  
2 faulty connection if the first RC constant is greater than the second RC constant.

1       7.     The method of claim 1, wherein performing the chip-to-package connectivity test  
2 comprises generating a transition signal from a driver of the common I/O, wherein the  
3 driver is configured as a weak driver.

1       8.     The method of claim 7, wherein generating the transition from the weak driver  
2 comprises placing an additional impedance into connection with the driver prior to  
3 launching the transition.

1       9.     The method of claim 8, wherein placing an additional impedance into connection  
2 with the driver comprises placing a resistor into series connection with the driver.

1       10.    The method of claim 8, further comprising electrically shorting the additional  
2 impedance from connection with the driver after launching the transition.

1       11.    The method of claim 10, wherein electrically shorting the additional impedance  
2 includes completing a circuit around the additional impedance to bypass the additional  
3 impedance.

1       12. A method of reduced pin count testing the chip-to-package connectivity of a  
2 semiconductor device, the method comprising:  
3 launching a transition from a common I/O driver on the packaged semiconductor device;  
4 observing a response of the transition at a point within the semiconductor device;  
5 determining whether a chip-to-package connection associated with the I/O is faulty from  
6 the response of the transition.

1       13. The method of claim 12, further comprising driving the transition with a weak  
2 driver.

1       14. An apparatus configured to launch a test signal to a common I/O of a  
2 semiconductor device from a driver on the semiconductor device which is associated with  
3 the common I/O using reduced pin count testing, the apparatus comprising:  
4       a test fixture configured to couple to a common I/O of the semiconductor device;  
5       a weak driver impedance coupled between the driver and the test fixture;  
6       wherein the apparatus is configured to launch the test signal through the weak  
7 driver impedance and the common I/O to the test fixture and evaluate a characteristic of a  
8 response to the test signal to determine whether a chip-to-package connection associated  
9 with the common I/O is faulty.

1       15. The apparatus of claim 14, wherein the weak driver impedance includes at least  
2 one of a switchable impedance and a variable impedance.

1       16. The apparatus of claim 14, wherein the weak driver impedance is an impedance  
2 having a resistive value of 1 K $\Omega$  or more.

1       17. The apparatus of claim 16, wherein the weak driver impedance is approximately  
2 10 K $\Omega$  or more.

1       18.     The apparatus of claim 14, further comprising a fixture impedance coupled  
2     between the test fixture and at least one of the semiconductor device and a potential  
3     relative to the semiconductor device.

1       19.     The apparatus of claim 18, wherein the fixture impedance comprises a capacitor  
2     coupled between the common I/O and a fixed potential relative to the semiconductor  
device.

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